

Clock and Data Recovery for 10-Gb/s EPON Application

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Abstract: An integrated 10-Gb/s clock and data recovery circuit incorporates a LC-tank voltage-controlled oscillator, a half-rate binary phase detector and charge pump. On the basis of R.C.Walker's second-order model, and in accordance with jitter tolerance and jitter transfer, the minimum stability factor are derived in a view to determine the value of C_z and R_z finally. After the circuit design is accomplished in 0.13- μm CMOS process, the power consumption is 210 mW from a supply voltage of 1.2V. When 10.125 Gb/s pseudorandom binary sequence is used, the jitter of the recovered clock is a peak-to-peak jitter of 8 ps.

Keywords: CDR, VCO, PD, CP, Jitter tolerance, Jitter transfer.

1. INTRODUCTION

With the development of optical fiber and multimedia communication, people have higher requirements for communication quality. Among numerous Passive Optical Network architectures, 10Gbit/s Ethernet Passive Optical Network (EPON) in IEEE 802.3av protocol is one of the most popular architectures [1]. CDR is the most important module in 10G-EPON, and there are multiple approaches to completing the module function, such as PLL-Based CDR [2-4], PI-Based CDR [5], Injection Locking [6, 7], Gated VCO [8], Oversampling [9]. Among them, based on difference of PD in PLL structure, they rare divided into structures of binary phase detector [10] and linear phase detector. The former has higher gains and has inhibited periodic jitter, but due to the nonlinear structure of PD, it is difficult to analyze and design. At present, there have been two classic analysis models used to deal with CDR of this kind of structure, one of which is based on the Jri. Lee's [11, 12] piecewise linear model of large-signal, and another one is R.C. Walker's [13] Δ - Σ model. The former is mainly used for relatively rough estimation, while the latter can calculate the upper limit of maximum capacitance value that the module requires.

In this paper, on the basis of R.C. Walker's second-order Δ - Σ model, and requirements of jitter tolerance and jitter transfer in 802.3av protocol, derives the minimum stability factor and the scope of stepped frequency, then coupled with charge pump current and the gain of VCO, calculates the minimum value C_z and the resistance R_z so as to complete circuit design.

2. CDR LOOP ANALYSIS

2.1. CDR Architecture

The CDR architecture includes a bang-bang PD, a charge pump, a low pass filter and an integrated LC-tank VCO, as shown in Fig. (1). The second-order CDR [13] can be rendered into a block diagram for analysis as shown in Fig. (2). $\Delta\omega$, is defined as the difference between the data frequency and the VCO frequency. And at the same time, the incoming data signal has a zero mean phase jitter of $\varphi(t)$.

It can be got from Fig. 1 that $V_{ctrl} = I_{cp}(R_z + 1/sC_z) = I_{cp}R_z + I_{cp}/sC_z$, and then input voltage of VCO, $\beta + K_{cp}/s$ can be deduced by contrasting Fig. (2), thereby

$$\beta = I_{cp} \cdot R_z \quad (1)$$

$$K_{cp} = \frac{I_{cp}}{C_z} \quad (2)$$

As can be seen from the Fig. (2), it contains the integral frequency control loop and the proportional phase control loop. The output voltage of the former causes the output frequency of the VCO to be changed ω_{int} on the basis of its free oscillation frequency. Therefore, the second - order CDR can dynamically track the change of input frequency, which broadens the frequency-locking range of CDR loop.

2.2. Stability Factor

The loop phase change in one update time due to the proportional connection is $\theta_{bb} = \omega_{bb}t_n = \beta K_{vco}t_n$. The phase

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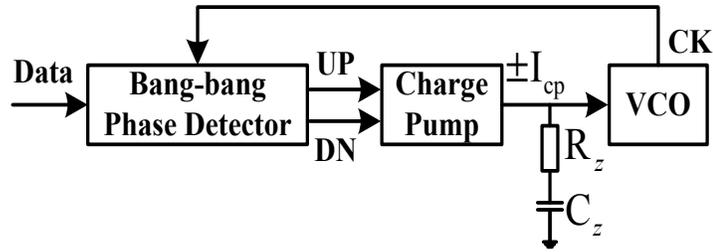


Fig. (1). Half-rate CDR Architecture.

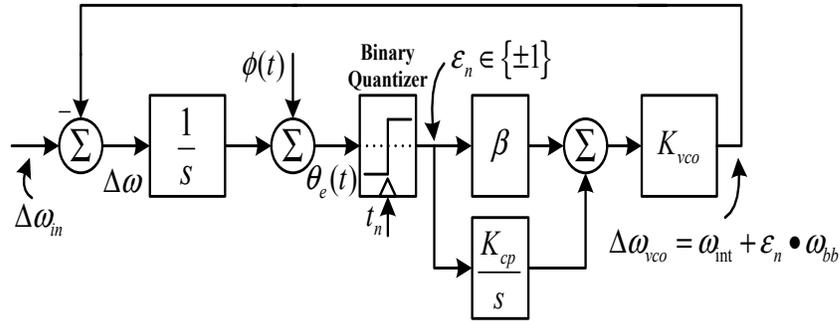


Fig. (2). Δ-Σ Model of second-order CDR.

change due to the integral branch is $\theta_{int} = \int_0^{t_n} \omega_{int} dt = \int_0^{t_n} (K_{cp} t) K_{vco} dt = K_{cp} K_{vco} t_n^2 / 2$. So the phase change in total circuit is given by

$$\theta_v(t) = \theta_{bb} + \theta_{int} = \omega_{bb} t + \frac{K_{cp} K_{vco} t^2}{2} \quad (3)$$

The ratio of these two is the stability factor of the loop

$$\xi = \frac{\theta_{bb}}{\theta_{int}} = \frac{2\beta}{K_{cp} t_n} \quad (4)$$

The integral frequency control loop has increased the risk of the stability of loop, which may result in the over-shoot of output phase $\theta_v(t)$. In order to ensure the stability of second-order CDR loops, R. C. Walker requires as to the stability factor of the loops, and at this point, the impact of proportion circuit on the output phase $\theta_v(t)$ has been predominated.

Assuming that the second-order CDR loop is locked at first, then a step signal θ_{step} is given to the phase of the input data $\theta_d(t)$, and the loop can't track the change of input phase. At this moment, PD outputs 1 is continuous. Output phase $\theta_v(t)$ in time domain is given by

$$\theta_v(t) = \theta_{bb} + \theta_{int} = \omega_{bb} (t + \frac{t^2}{\xi t_n}) \quad (5)$$

The time experienced from output phase $\theta_v(t)$ tacking into the input phase $\theta_d(t)$ is

$$t_1 = \frac{\sqrt{1 + \frac{4\theta_{step}}{\xi\theta_{bb}} - 1}}{2} \quad (6)$$

After t_1 , as long as the proportional phase control loop plays a main role, there won't be over-shoot of phase in system, thereby

$$\omega_{int}(t_1) = \omega_{bb} \frac{2t_1}{\xi t_n} \leq \omega_{bb} \quad (7)$$

The minimum value of the stability factor is solved when over-shoot of phase phenomenon never occurs in system. The minimum value of the stability factor is given by

$$\xi \geq \frac{4\theta_{step}}{3\theta_{bb}} \quad (8)$$

2.3. The Jitter Tolerance

According to the stability factor of the loop, R. C. Walker has derived the condition when slope overload never occurs in second-order loop

$$\omega(s) \leq \omega_{bb} (1 + \frac{1}{s + \omega_{bb}}) \frac{2\omega_{bb}}{s\xi} \quad (9)$$

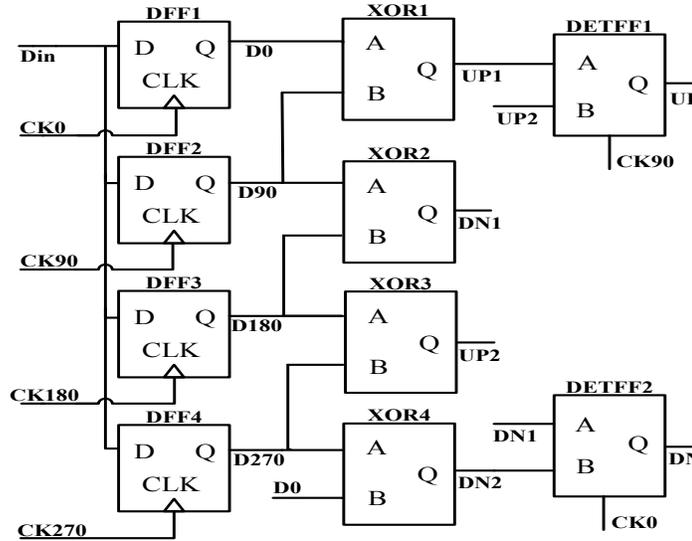


Fig. (3). Phase Detector.

Assumed that the frequency of input data does not change, but it is modulated by a sine signal in input phase $\varphi(t)$, and the input phase $\varphi(t) = m_j \sin(2\pi f_j t_n + \varphi_j)$ is namely sine jitter. Where m_j is amplitude of sinusoidal jitter; f_j is the frequency of jitter; φ_j is its initial phase. Supposed that the condition of the jitter tolerance is that slope overload doesn't occur in system, it can be obtained that

$$m_j \cdot s \Big|_{s=j2\pi f_j} \leq \omega_{bb} \left(1 + \frac{1}{s + \omega}\right) \frac{2\omega_{bb}}{s\xi} \quad (9)$$

Generally speaking, $|s| \gg 2/\xi$, equivalently, by

$$\omega_{bb} \geq m_j \cdot 2\pi f_j \quad (10)$$

2.4. The Jitter Transfer

When slope overload doesn't occur in the system, the output phase of the second-order CDR loop can accurately track the change of input phase. Similarly, assume that the slope overload just occur in the system, the loop bandwidth is namely the bandwidth of jitter transfer, $BW_{JT} = \omega_{bb_JT} / 2\pi m_j$. Based on the fact that the loop bandwidth of design circuit is required to be smaller than the bandwidth of the jitter transfer curve, can be derived that

$$\omega_{bb} \leq BW_{JT} 2\pi m_j \quad (11)$$

3. CIRCUIT DESIGN

3.1. Phase Detector

Phase detector can be classified into linear PDs and Binary PDs. Because the former generate a linearly proportional output with phase error, it is less suitable for high

speed circuit. Binary PDs only care about the phase lead or the phase lag, producing a positive or negative value at their output. Therefore, a half-rate binary PD was applied. The block diagram of the phase detector circuit is shown in Fig. (3). The data rate of CDR arrives to 10Gbps, so the DFF and other high speed parts were both implemented in current mode logic (CML).

PD received four clock signals from PLL. D0, D90 and D180 constitute the first set of sampling data three times in succession, and after exclusive-OR gate of XOR1 and XOR2, UP1 and DN1 signal outputted respectively. The signals of UP2 and DN2 are outputted in the same way. Double edge trigger (DEFF) is composed of two flip-latches and a demultiplexer, and solved the error of output because of signal delay. Finally, UP is outputted by signals of UP1 and UP2 after passing through DEFF1, while DN is outputted by signals of DN1 and DN2 after passing through DEFF2. Because operations of separate half-rate clock signals of CK0 and CK90 are implemented twice on DEFF1 and DEFF2 in one clock period, the updated frequency of their output signal of UP and DN is exactly the same as the full rate of Alexander phase discriminator.

3.2. Charge Pump

Fig. (4) shows the implementation of the differential charge pump. To be robust against supply and substrate noise, differential architecture was chosen. The entire same discharge and charge circuit is achieved by symmetric pump circuit. When the signal of DN+ or UP+ change from open state to closed state, parasitic capacitance of points of A and B causes slower rise of their electrical level, slowing down the operating speed of the circuit. A current mirror with smaller current value can be added to avoid this situation.

When the CDR is locked, the PD circuit generates no pulses, the filter capacitance is discharged by the impedances of the current sources and by currents caused by current source mismatches. To reduce both effects, the cascode current sources are used, at the same time, M1 and M2 need to

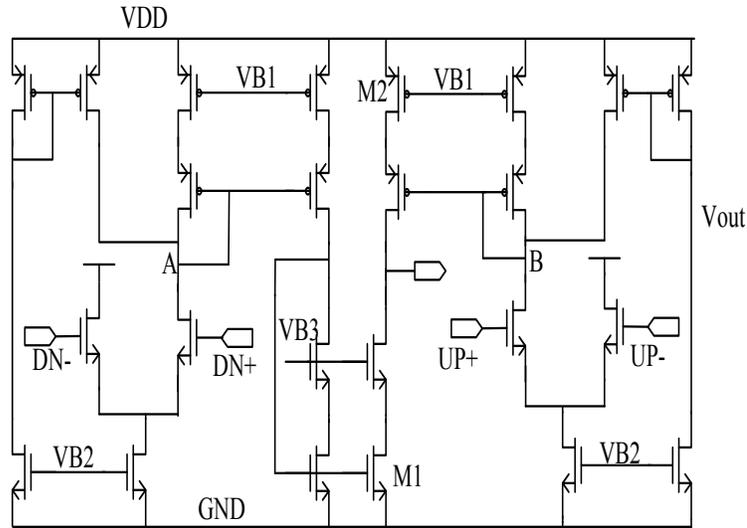


Fig. (4). Charge pump.

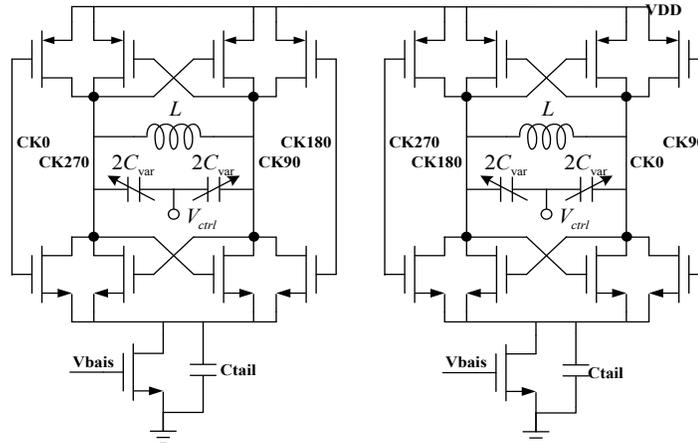


Fig. (5). Schematic of VCO.

choose a large dimension. The variations of V_{th} may result in current source mismatches and V_{th} are roughly proportional to the square root of the gate area. So a large gate area can reduce current mismatch.

3.3. Loop Filter

The performance of CDR loop is decided by loop filter. Through the above analysis of CDR second-order loop, and according to the jitter requirements by agreement, stepped frequency ω_{bb} and stability factor ζ , coupled with the current I_{cp} of CP and the gain K_{vco} of VCO can be obtained. By $\omega_{bb} = \beta K_{vco} = I_{cp} R_z K_{vco}$ and $\zeta = \theta_{bb} / \theta_{int} = 2\beta / K_{cp} t_n$, the parameters of the loop filter are given by

$$R_z = \frac{\omega_{bb}}{I_{cp} K_{vco}} \tag{12}$$

$$C_z = \frac{\zeta t_n}{2R_z} \tag{13}$$

3.4. VCO

The design of the VCO directly impacts the jitter performance and the reproducibility of the CDR circuit. A ring oscillator is an easy design and low-cost, but it is difficult to achieve a potentially lower jitter. To reduce phase noise, LC topologies was applied.

Fig. (5) shows the implementation of the QVCO. Cross coupling of PMOS and PMOS transistor is conducted, which has reduced the tail current of QVCO and the power consumption of the circuit when start-oscillating condition is satisfied. At the same time, rising edge of output waveform is more symmetrical with its falling edge, because the PD is half rate. Parallel-coupled can achieve the clock output of quadrature phase. A capacitance is connected in parallel with

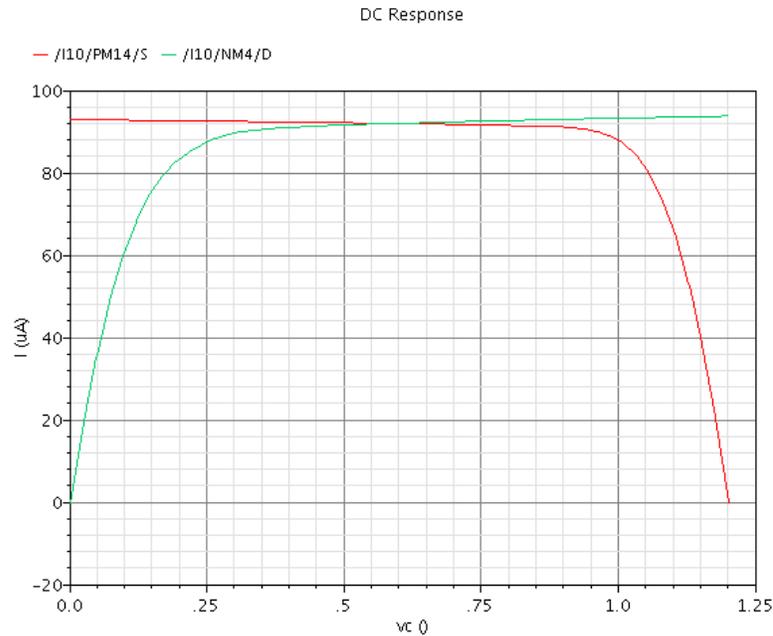


Fig. (6). Simulated Current mismatch of CP.

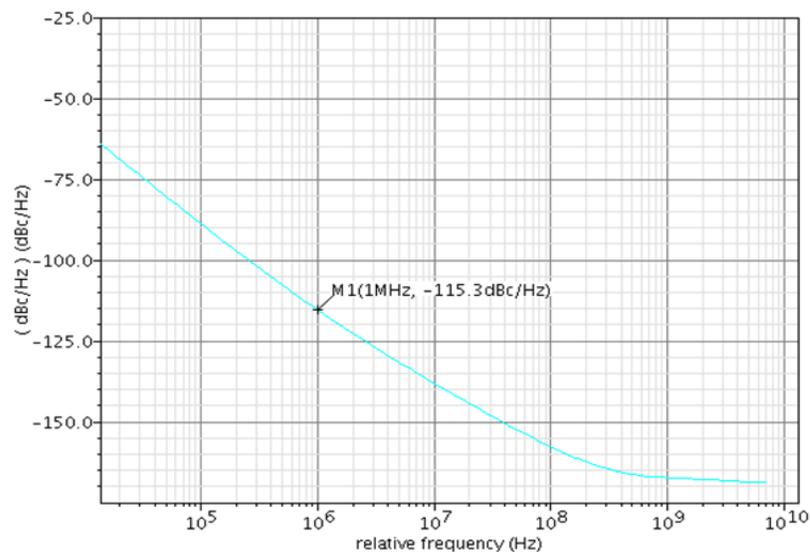


Fig. (7). Simulated Phase Noise of VCO.

tail current source to reduce the amplitude of even-order harmonic.

4. SIMULATION RESULT

The CDR circuit has been designed in a 0.13 um CMOS process. The circuit mismatch of charge pump is shown in Fig. (6). The CP output voltage increased from 0.43V to 0.78V when mismatch current is less than 1uA.

VCO is an extremely significant module in CDR, and its jitter performance is directly related to the recovered data. The simulation curve of phase noise of VCO is shown in Fig.

(7), when the center frequency is 5.1 GHz, the phase noise at 1 MHz is -115.3dBc/Hz.

The CDR was simulated with a pseudo-random bit sequence (PRBS) of length $2^{23} - 1$. The rate of input data is 10 G/s. The eye diagram of clock signal recovered by CDR is as shown in Fig. (8), with a peak - to - peak jitter of 8ps.

CONCLUSION

Low-cost, low-power, and high-integration issues make CMOS the preferred technology for high-speed optical communication circuits. A 10-Gb/s clock and data recovery

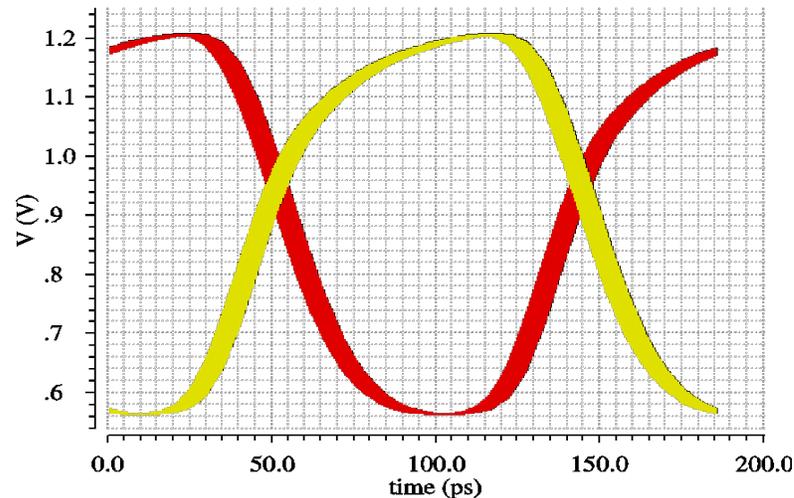


Fig. (8). Simulated recovered clock.

circuit designed in 0.13- μ m CMOS technology performs phase locking, data regeneration.

CONFLICT OF INTEREST

The authors confirm that this article content has no conflicts of interest.

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Declared none.

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